CLAIMS

What is claimed is:

1. A method of handling memory errors comprising:
receiving a memory fault indication that is true if an error in the memory is detected while executing a memory load request to retrieve a value from the memory;
receiving a speculative load indication that is true if the memory load request was issued speculatively; and
if the memory fault indication is true and the speculative load indication is true,
providing an error indication that the returned value is invalid,
otherwise,
performing error recovery.

2. The method of claim 1, wherein the error indication is a flag bit associated with the returned value.

3. The method of claim 1, wherein the error indication is setting the returned value to an invalid value.

4. The method of claim 1, further comprising receiving a fault deferral indication that is true if faults can be deferred, wherein providing an error indication is performed if, in addition to the memory fault indication being true and the speculative load indication being true, the fault deferral indication is true.

5. The method of claim 1, wherein providing an error indication is performed if, in addition to the memory fault indication being true and the speculative load indication being true, the error in the memory is uncorrectable.

6. A machine-readable medium that provides instructions, which when executed by a machine, cause the machine to perform operations comprising:

receiving a memory fault indication that is true if an error in the memory is detected while executing a memory load request to retrieve a value from the memory;

receiving a speculative load indication that is true if the memory load request was issued speculatively; and

if the memory fault indication is true and the speculative load indication is true,

providing an error indication that the returned value is invalid,

otherwise,

performing error recovery.

7. The machine-readable medium of claim 6, wherein the error indication is a flag bit associated with the returned value.

8. The machine-readable medium of claim 6, wherein the error indication is setting the returned value to an invalid value.

9. The machine-readable medium of claim 6, further comprising receiving a fault deferral indication that is true if faults can be deferred, wherein providing an error indication is performed if, in addition to the memory fault indication being true and the speculative load indication being true, the fault deferral indication is true.

10. The machine-readable medium of claim 6, wherein providing an error indication is performed if, in addition to the memory fault indication being true and the speculative load indication being true, the error in the memory is uncorrectable.

11. A machine comprising:
an interface to receive a value from a memory coupled to the machine;
a memory fault indicator that is true if an error in the memory is detected while executing a memory load request to retrieve a value from the memory;
a speculative load indicator that is true if the memory load request was issued speculatively; and
a machine-readable medium that provides instructions, which when executed by a machine, cause the machine to perform operations including
if the memory fault indicator is true and the speculative load indicator is true,
providing an error indication that the returned value is invalid, otherwise,
performing error recovery.

12. The machine of claim 11, wherein the machine further comprises a register to receive the value, and a flag bit associated with the register, wherein the error indication is a defined value of the flag bit.

13. The machine of claim 11, wherein the machine further comprises a register to receive the value, and the error indication is an invalid value in the register.

14. The machine of claim 11, further comprising receiving a fault deferral indicator from the machine to indicate that faults can be deferred, wherein providing an error indication is performed if, in addition to the memory fault indicator being true and the speculative load indicator being true, the fault deferral indicator is true.

15. The machine of claim 11, wherein providing an error indication is performed if, in addition to the memory fault indication being true and the speculative load indication being true, the error in the memory is uncorrectable.

16. A system comprising:
a machine;
a memory coupled to the machine; and
a machine-readable medium that provides instructions, which when executed by the machine, cause the machine to perform operations including
receiving a memory fault indication that is true if an error in the memory is detected while executing a memory load request to retrieve a value from the memory,
receiving a speculative load indication that is true if the memory load request was issued speculatively, and
if the memory fault indication is true and the speculative load indication is true,
providing an error indication that the returned value is invalid,
otherwise,
performing error recovery.

17. The system of claim 16, wherein the machine further comprises a register to receive the value, and a flag bit associated with the register, wherein the error indication is a defined value of the flag bit.

18. The system of claim 16, wherein the machine further comprises a register to receive the value, and the error indication is an invalid value in the register.

19. The system of claim 16, further comprising receiving a fault deferral indicator from the machine to indicate that faults can be deferred, wherein providing an error indication is performed if, in addition to the memory fault

indicator being true and the speculative load indicator being true, the fault deferral indicator is true.

20. The system of claim 16, wherein providing an error indication is performed if, in addition to the memory fault indication being true and the speculative load indication being true, the error in the memory is uncorrectable.